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1 Robustness: Defensive programming: using an annotation toolkit to build DoS-resistant software ■
Xiaohu Qie, Ruoming Pang, Larry Peterson
December 2002 **ACM SIGOPS Operating Systems Review**, Volume 36 Issue SI

Full text available: 📄 pdf(2.13 MB)   Additional Information: full citation, abstract, references

> This paper describes a toolkit to help improve the robustness of code against DoS attacks. We observe that when developing software, programmers primarily focus on functionality. Protecting code from attacks is often considered the responsibility of the OS, firewalls and intrusion detection systems. As a result, many DoS vulnerabilities are not discovered until the system is attacked and the damage is done. Instead of reacting to attacks after the fact, this paper argues that a better solution i ...

2 Web-based and Java-based simulation: The MONARC toolset for simulating large network-distributed processing systems ■
Iosif C. Legrand, Harvey B. Newman
December 2000 **Proceedings of the 32nd conference on Winter simulation**

Full text available: 📄 pdf(467.46 KB)   Additional Information: full citation, abstract, references

> The next generation of High Energy Physics experiments have envisaged the use of network-distributed Petabyte-scale data handling and computing systems of unprecedented complexity. The general concept is that of a "Data Grid Hierarchy" in which the central facility at the European Laboratory for Particle Physics (CERN) in Geneva will interact and coherently manage tasks shared by and distributed amongst national "Tier1 (National) Regional Centres" situated in the US, Europe, and Asia. CERN and t ...

3 Saturn V Prelaunch Systems Simulation Model for a launch opportunity containing multiple launch windows ■
Bernard J. Schroer
December 1969 **Proceedings of the third conference on Applications of simulation**

Full text available: 📄 pdf(1.48 MB)   Additional Information: full citation, abstract, references, citings, index terms

> This paper presents the results of the Saturn V Prelaunch Systems Simulation Model for a launch opportunity containing multiple launch windows. The simulation consisted of the events in operation during the last 26 hours of the Saturn V countdown (i.e., T-26 hours to liftoff). The measure of effectiveness, Launch Vehicle Availability (LVA), was evaluated for various launch window configurations.

4 <u>Knowledge management: a new idea or a recycled concept?</u>
Israel Spiegler
June 2000 **Communications of the AIS**

Full text available: pdf(168.08 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>

5 <u>Hanford tank waste remediation system overview: a dynamic simulation model</u>
K. D. Boomer, R. S. Wittman, M. A. Duffy, C. M. Watson
December 1994 **Proceedings of the 26th conference on Winter simulation**

Full text available: pdf(597.20 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

6 <u>Superscalar design: Cherry: checkpointed early resource recycling in out-of-order microprocessors</u>
José F. Martínez, Jose Renau, Michael C. Huang, Milos Prvulovic, Josep Torrellas
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.40 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index</u>
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This paper presents *CHeckpointed Early Resource RecYcling (Cherry)*, a hybrid mode of execution based on ROB and checkpointing that decouples resource recycling and instruction retirement. Resources are recycled early, resulting in a more efficient utilization. Cherry relies on state checkpointing and rollback to service exceptions for instructions whose resources have been recycled. Cherry leverages the ROB to (1) not require in-order execution as a fallback mechanism, (2) allow memory re ...

7 <u>Automatic batch processing in multilayer ceramic metallization</u>
Neil DalCero
June 1983 **Proceedings of the 20th conference on Design automation**

Full text available: pdf(311.37 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>index terms</u>

This paper describes advances in the batch processing automation of multilayer ceramic metallization manufacturing. The metallization is a plating process that deposits electroless nickel and electroless gold on conductive molybdenum features. The plating operation involves the processing of up to 72 multilayer ceramic substrates in one group. Each product group automatically moves through 35 sequential chemical operations to complete the process. As a product is compl ...

8 <u>Graphic display techniques in the automated interconnection process</u>
R. R. Klemetsmo, G. A. Minturn, A. I. Wright
July 1968 **Proceedings of the 5th annual workshop on Design automation**

Full text available: pdf(674.52 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>index terms</u>

At present, it is necessary to negotiate a manual completion phase in wiring multi-layer interconnection boards used in aerospace computers. This phase occurs after automatic placement of logic modules and routing of the greater majority of the requisite wiring. The GAPE (Graphic Aids to Packaging Engineering) System utilizes an IBM 2250 to minimize not only time-consuming and error-prone functions in the wiring completion process but also the total amount of computer time required. Selecti ...

9 <u>Full Technical Papers: Multimodal event parsing for intelligent user interfaces</u>

Will Fitzgerald, R. James Firby, Michael Hannemann
January 2003 **Proceedings of the 8th international conference on Intelligent user interfaces**
Full text available: pdf(827.30 KB)　　Additional Information: full citation, abstract, references, index terms

Many intelligent interfaces must recognize patterns of user activity that cross a variety of different input channels. These multimodal interfaces offer significant challenges to both the designer and the software engineer. The designer needs a method of expressing interaction patterns that has the power to capture real use cases and a clear semantics. The software engineer needs a processing model that can identify the described interaction patterns efficiently while maintaining meaningful inte ...

Keywords: CERA, event recognition, multi-modal parsing

10 Performance analysis and optimization of latency insensitive systems
Luca P. Carloni, Alberto L. Sangiovanni-Vincentelli
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(235.41 KB)　　Additional Information: full citation, abstract, references, citings, index terms

Latency insensitive design has been recently proposed in literature as a way to design complex digital systems, whose functional behavior is robust with respect to arbitrary variations in interconnect latency. However, this approach does not guarantee the same robustness for the performance of the design, which indeed can experience big losses. This paper presents a simple, yet rigorous, method to (1) model the key properties of a latency insensitive system, (2) analyze the impact o ...

11 Recycling continuations
Jonathan Sobel, Daniel P. Friedman
September 1998 **ACM SIGPLAN Notices , Proceedings of the third ACM SIGPLAN international conference on Functional programming**, Volume 34 Issue 1

Full text available: pdf(1.35 MB)　　Additional Information: full citation, abstract, references, citings, index terms

If the continuations in functional data-structure-generating programs are made explicit and represented as records, they can be "recycled." Once they have served their purpose as temporary, intermediate structures for managing program control, the space they occupy can be reused for the structures that the programs produce as their output. To effect this immediate memory reclamation, we use a sequence of correctness-preserving program transformations, demonstrated through a series of simple exam ...

12 Specifying software/hardware interactions in distributed systems
G-C. Roman
March 1987 **Proceedings of the 9th international conference on Software Engineering**

Full text available: pdf(1.18 MB)　　Additional Information: full citation, abstract, references, citings, index terms

This paper describes a system level specification approach that enables the designer to formulate and answer questions regarding the system's logical correctness and performance characteristics when the interaction between the hardware and the software is important, i.e., when the impact of faults, failures, communication delay, hardware selection, scheduling policies, etc., must be considered. In the simplest terms, our concern extends beyond the traditional software correctness questions ...

13 Hybrid dynamic data race detection
Robert O'Callahan, Jong-Deok Choi

June 2003 **ACM SIGPLAN Notices , Proceedings of the ninth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 38 Issue 10

Full text available: pdf(158.47 KB)   Additional Information: full citation, abstract, references, citings, index terms

We present a new method for dynamically detecting potential data races in multithreaded programs. Our method improves on the state of the art in accuracy, in usability, and in overhead. We improve accuracy by combining two previously known race detection techniques -- *lockset-based detection and happens-before-based detection* -- to obtain fewer false positives than lockset-based detection alone. We enhance usability by reporting more information about detected races than any previous dyna ...

Keywords: Java, dynamic race detection, happens-before, lockset hybrid

14 Making the annual CHI conference environmentally sound

Rory Stuart, Shelly Dews
January 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 1

Full text available: pdf(293.09 KB)   Additional Information: full citation, index terms

15 Applications II: A compiled accelerator for biological cell signaling simulations

John F. Keane, Christopher Bradley, Carl Ebeling
February 2004 **Proceeding of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

Full text available: pdf(191.01 KB)   Additional Information: full citation, abstract, references, index terms

The simulation of large systems of biochemical reactions is a key part of research into molecular signaling and information processing in biological cells. However, it can be impractical because many relevant reactions are modeled as stochastic, discrete event processes, and the complexity of the computing task scales with the number of discrete events in a simulation. Traditionally, such simulations are computed on general purpose CPUs, and sometimes in networks of such processors. We show that ...

Keywords: biology, cell, reactions, reconfigurable hardware, simulation

16 Space-time memory: a parallel programming abstraction for interactive multimedia applications

Umakishore Ramachandran, Rishiyur S. Nikhil, Nissim Harel, James M. Rehg, Kathleen Knobe
May 1999 **ACM SIGPLAN Notices , Proceedings of the seventh ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 34 Issue 8

Full text available: pdf(1.28 MB)   Additional Information: full citation, abstract, references, citings, index terms

Realistic interactive multimedia involving vision, animation, and multimedia collaboration is likely to become an important aspect of future computer applications. The scalable parallelism inherent in such applications coupled with their computational demands make them ideal candidates for SMPs and clusters of SMPs. These applications have novel requirements that offer new kinds of challenges for parallel system design.We have designed a programming system called *Stampede* that offers many ...

17 A space logistics simulation implementation in Ada

Jesus Borrego, Frank Cheng, Ron Janz
December 1988 **Proceedings of the 20th conference on Winter simulation**

Full text available: 📄 pdf(405.38 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

This paper describes some of the issues involved in converting a prototype of a large-scale discrete event simulation written in SIMSCRIPT 11.5 and FORTRAN into Ada. Specific features provided by SIMSCRIPT that needed to be created in Ada are discussed. Preliminary conclusions regarding the use of both languages for large-scale simulations are then presented.

18 <u>What are race conditions?: Some issues and formalizations</u>
Robert H. B. Netzer, Barton P. Miller
March 1992 **ACM Letters on Programming Languages and Systems (LOPLAS)**, Volume 1
Issue 1

Full text available: 📄 pdf(1.16 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>, <u>review</u>

In shared-memory parallel programs that use explicit synchronization, race conditions result when accesses to shared memory are not properly synchronized. Race conditions are often considered to be manifestations of bugs, since their presence can cause the program to behave unexpectedly. Unfortunately, there has been little agreement in the literature as to precisely what constitutes a race condition. Two different notions have been implicitly considered: one pertaining to ...

Keywords: critical sections, data races, debugging, nondeterminacy, parallel programs, race conditions

19 <u>SEDA: an architecture for well-conditioned, scalable internet services</u>
Matt Welsh, David Culler, Eric Brewer
October 2001 **ACM SIGOPS Operating Systems Review , Proceedings of the eighteenth ACM symposium on Operating systems principles**, Volume 35 Issue 5

Full text available: 📄 pdf(1.51 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

We propose a new design for highly concurrent Internet services, which we call the *staged event-driven architecture* (SEDA). SEDA is intended to support massive concurrency demands and simplify the construction of well-conditioned services. In SEDA, applications consist of a network of event-driven *stages* connected by explicit *queues*. This architecture allows services to be well-conditioned to load, preventing resources from being overcommitted when demand exceeds service cap ...

20 <u>Processor self-scheduling in parallel discrete event simulation</u>
Pavlos Konas, Pen-Chung Yew
December 1995 **Proceedings of the 27th conference on Winter simulation**

Full text available: 📄 pdf(794.22 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

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